Introduction to the x86 Architecture

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September 29, 2015

vms Software

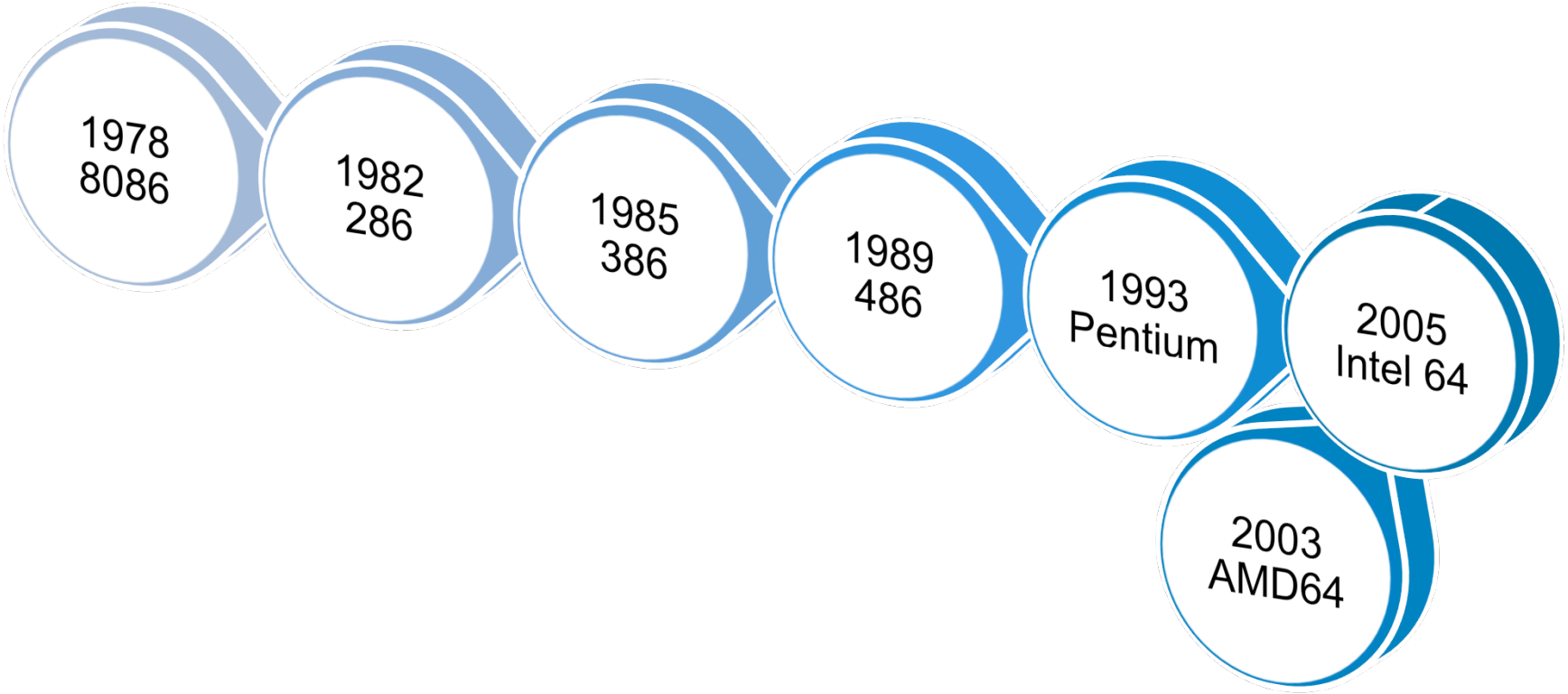
Introduction to the x86 Architecture

This information contains forward looking statements and is provided solely for your convenience. While the information herein is based on our current best estimates, such information is subject to change without notice.

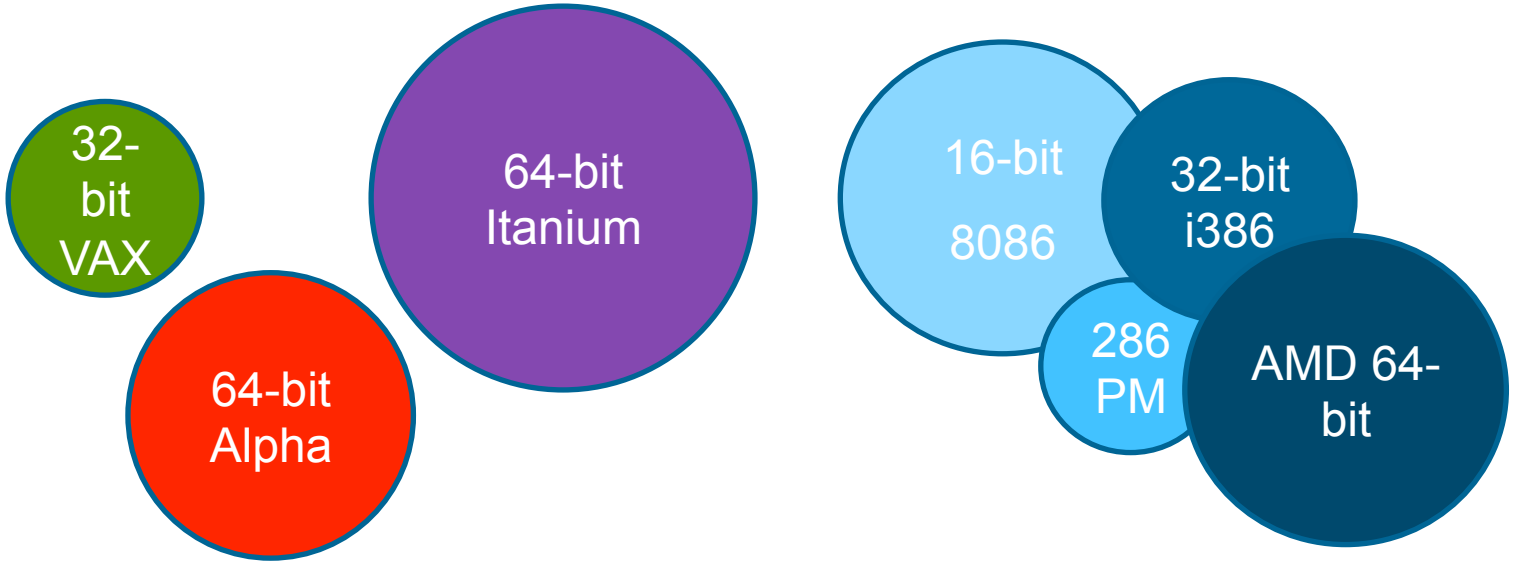
x86 Heritage

Comparison at a Glance
CPU Design Strategy
Register Set
Instruction Encoding
Memory Layout
VMS
RAS Features
Proliferation of x86

x86 Development Timeline



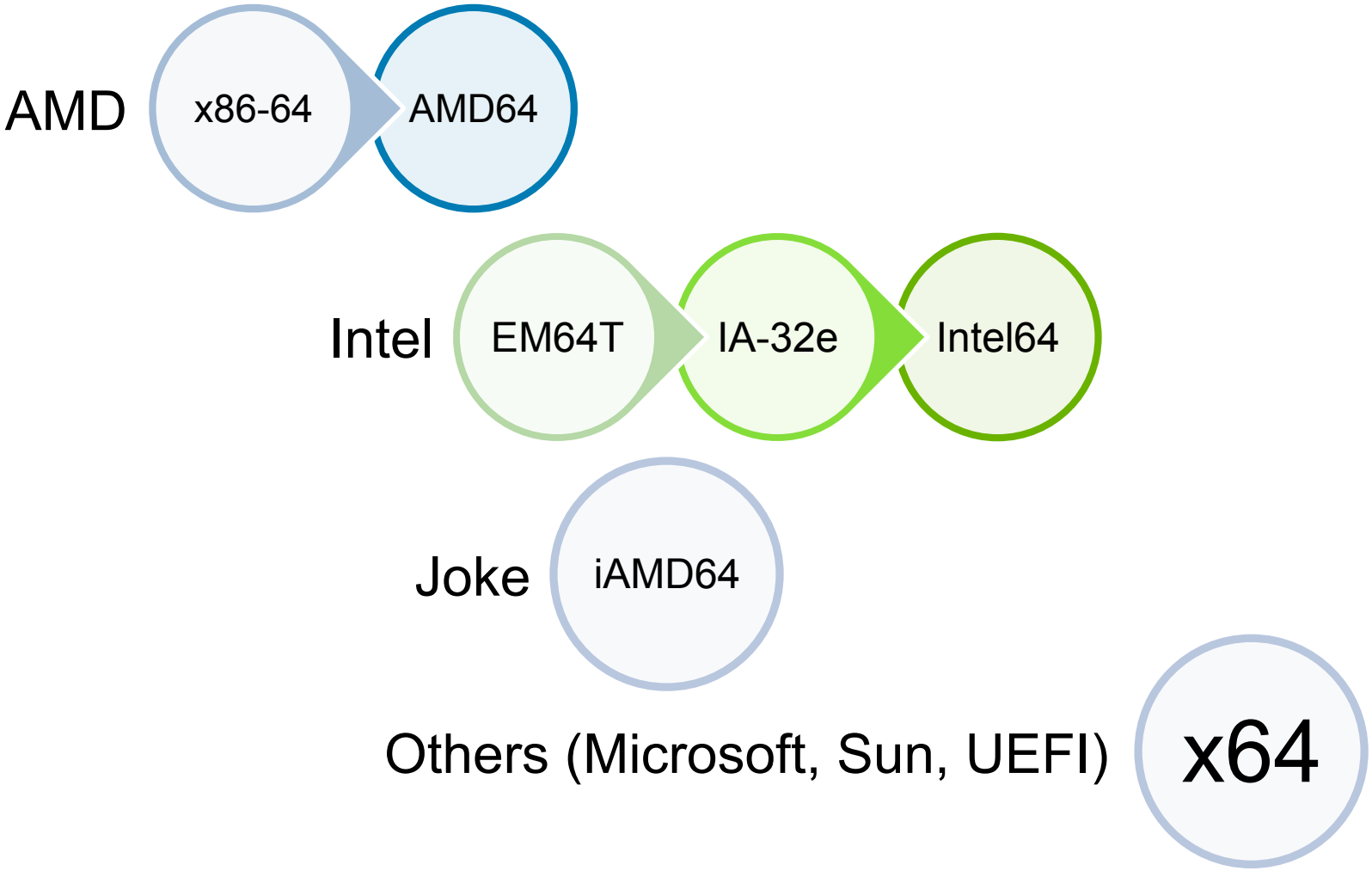
New Designs vs Extensions



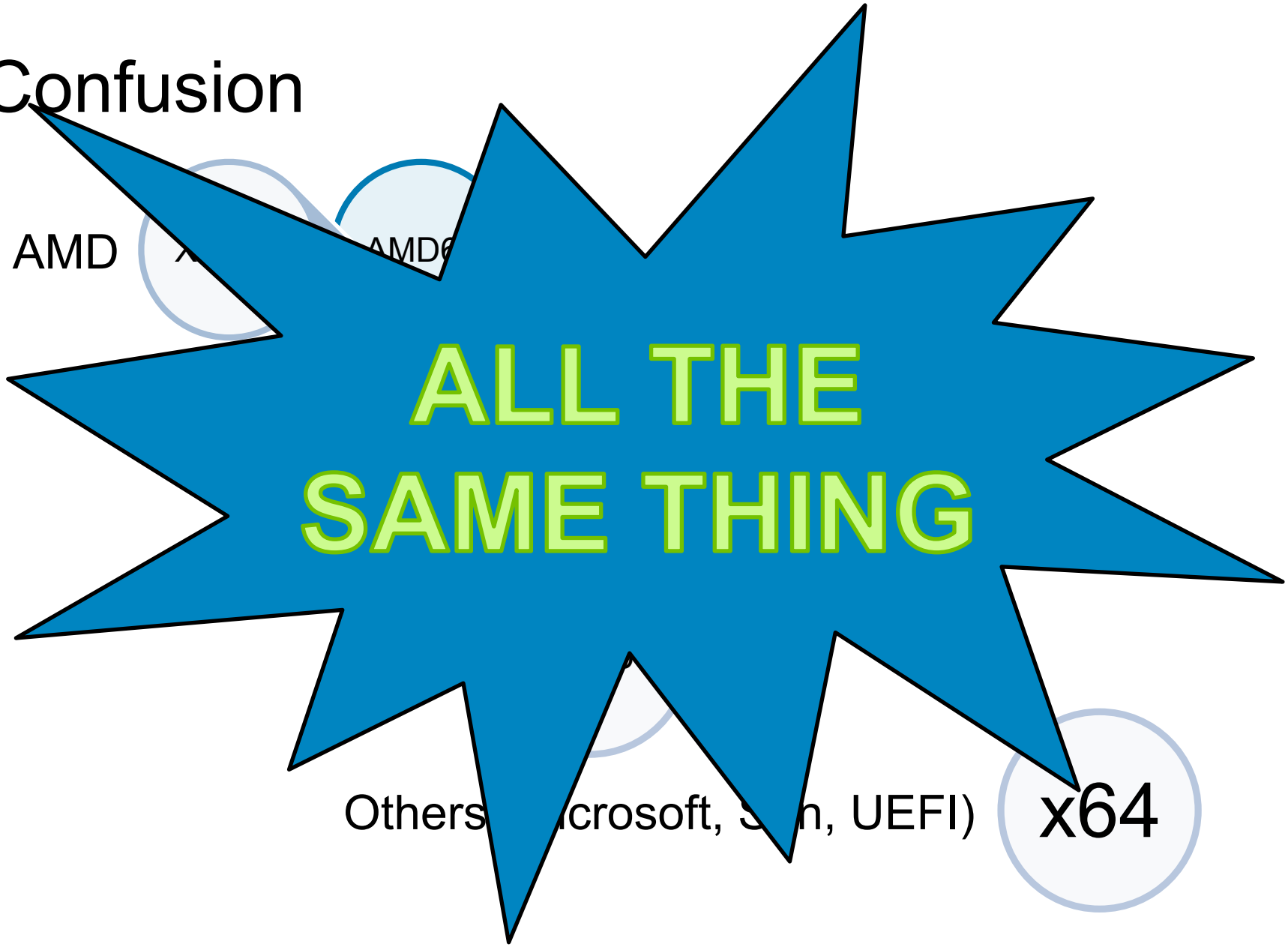
Nomenclature

Architecture	Sub-arch.	First in	Other implementations
x86 (16-bit)	8086	8086	8088, V20, V30, 80186
	i286	80286	
IA-32 (32-bit)	i386	80386	Am386
	i486	80486	Am486
	i586	Pentium	Pentium MMX, K5, K6
	i686	Pentium Pro	Pentium II, Pentium III, Pentium 4, Athlon
x86-64 (64-bit)	AMD64	Opteron	Athlon 64, Turion, Sempron, Phenom
	Intel 64	Xeon	Pentium 4 “F”, Celeron, Core

Confusion


AMD
x86-64
AMD64
Intel
EM64T
IA-32e
Intel64
Joke
iAMD64
Others (Microsoft, Sun, UEFI)
x64

Confusion



Chip brand names and generations

- Intel64 brands
  - Xeon
  - Core
  - Pentium
  - Celeron
  - Atom
  - Quark
- AMD64 brands
  - Opteron
  - Athlon
  - Sempron
  - FX
  - A-Series
- Intel64 microarchitectures
  - Core, Penryn
  - Nehalem, Westmere
  - Sandy Bridge, Ivy Bridge
  - Haswell, Broadwell
  - Skylake
- AMD64 microarchitectures
  - K8 Hammer, K10, Fusion
  - Bobcat, Jaguar, Puma
  - Bulldozer, Piledriver, Steamroller, Excavator
  - Zen

ISA Extensions

Name	First in	Function
x87	8086+8087 (1980)	Floating Point Co-processor
PM	80286 (1982)	Protected Mode: Virtual Memory
IA-32	80386 (1985)	32-bit
PAE	Pentium Pro (1995)	Physical Address Extension
MMX	Pentium MMX (1997)	MultiMedia Extension (Integer SIMD)
3Dnow!	AMD K6-2 (1998)	3D Graphics (Floating Point SIMD)
SSE(n)	Pentium III (1999)	Streaming SIMD Extensions (FP SIMD)
x86-64	Opteron (2003)	64-bit
VT-x	Pentium 4 (2005)	Virtualization support
AMD-V	Athlon 64 (2006)	Virtualization support
AES-NI	Westmere (2010)	Advanced Encryption Standard
AVX(n)	Sandy Bridge (2011)	Advanced Vector Extensions (FP SIMD)
TSX	Haswell (2013)	Transactional Synchronization Extension
MPX	Skylake (2015)	Memory Protection Extensions

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Some Numbers

	VAX	Alpha	Itanium2	x86
Word size	32	64	64	64
Architecture	CISC	RISC	EPIC	CISC*
Manufacturer	DEC	DEC	Intel	Intel AMD VIA
GP Registers	16	32+32(FP)	128+128(FP)	16+8(MMX)+16(XMM)
Orthogonality	YES	YES	-	-
Instructions	~460	~135	~150	>600**
Addr. Modes	24	4	6	10
Instr. size	8-400 bits	32 bits	41b (3/128b)	8-120 bits
transistors	1.3M (NVAX)	130M (EV7)	3.1B (Poulson***)	5.6B (E7-v3****)

* With an underlying RISC-Like core
** Depending on how you count them
*** 8 cores
**** 15 cores

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Traditional CISC Architecture (VAX)

- Complex Instruction Set Computer
- Complex instructions, mixing computation and memory access
- Microcoded implementations
- Makes optimizing code execution by the processor difficult

RISC Architecture (Alpha)

- Reduced Instruction Set Computer
- Simple instructions, separating computation and memory access
- Hardwired
- Relatively easily optimized by processor (parallel execution, re-ordering, pipelining, branch prediction, but…
- Optimization hardware becoming increasingly complex

EPIC Architecture (Itanium)

- Explicitly Parallel Instruction Set Computer
- Simple instructions, separating computation and memory access
- Parallel execution of instruction groups, separated by compiler-inserted stops.
- Predication instead of conditional branching
- Mostly hardwired
- Burden of optimization shifted to compiler (though Poulson fixes that by doing some reordering)

Modern CISC Architecture (x86)

- Complex instructions are translated into RISC-like micro-ops
- Partly hardwired
- Extensive optimization performed by processor (parallel execution, re-ordering, pipelining, branch prediction) after translation to micro-ops

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VAX Register Set

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
AP/R12
FP/R13
SP/R14
PC/R15

PSL
IPR’s

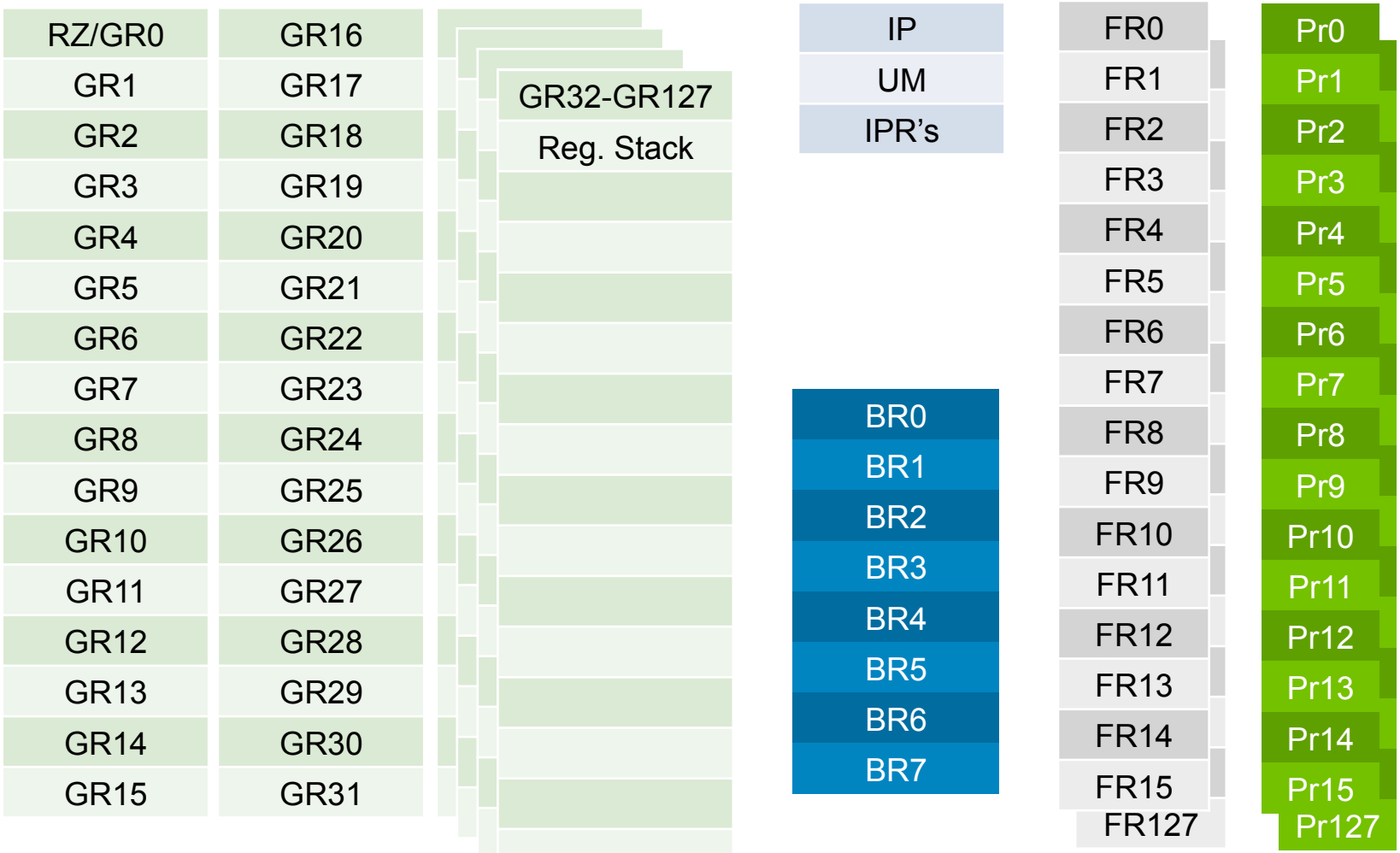
Alpha Register Set

R0	R16
R1	R17
R2	R18
R3	R19
R4	R20
R5	R21
R6	R22
R7	R23
R8	R24
R9	AI/R25
R10	RA/R26
R11	PV/R27
R12	R28
R13	FP/R29
R14	SP/R30
R15	RZ/R31

PC
PS
IPR's

F0	F16
F1	F17
F2	F18
F3	F19
F4	F20
F5	F21
F6	F22
F7	F23
F8	F24
F9	F25
F10	F26
F11	F27
F12	F28
F13	F29
F14	F30
F15	F31

Itanium Register Set



x86 Register Set

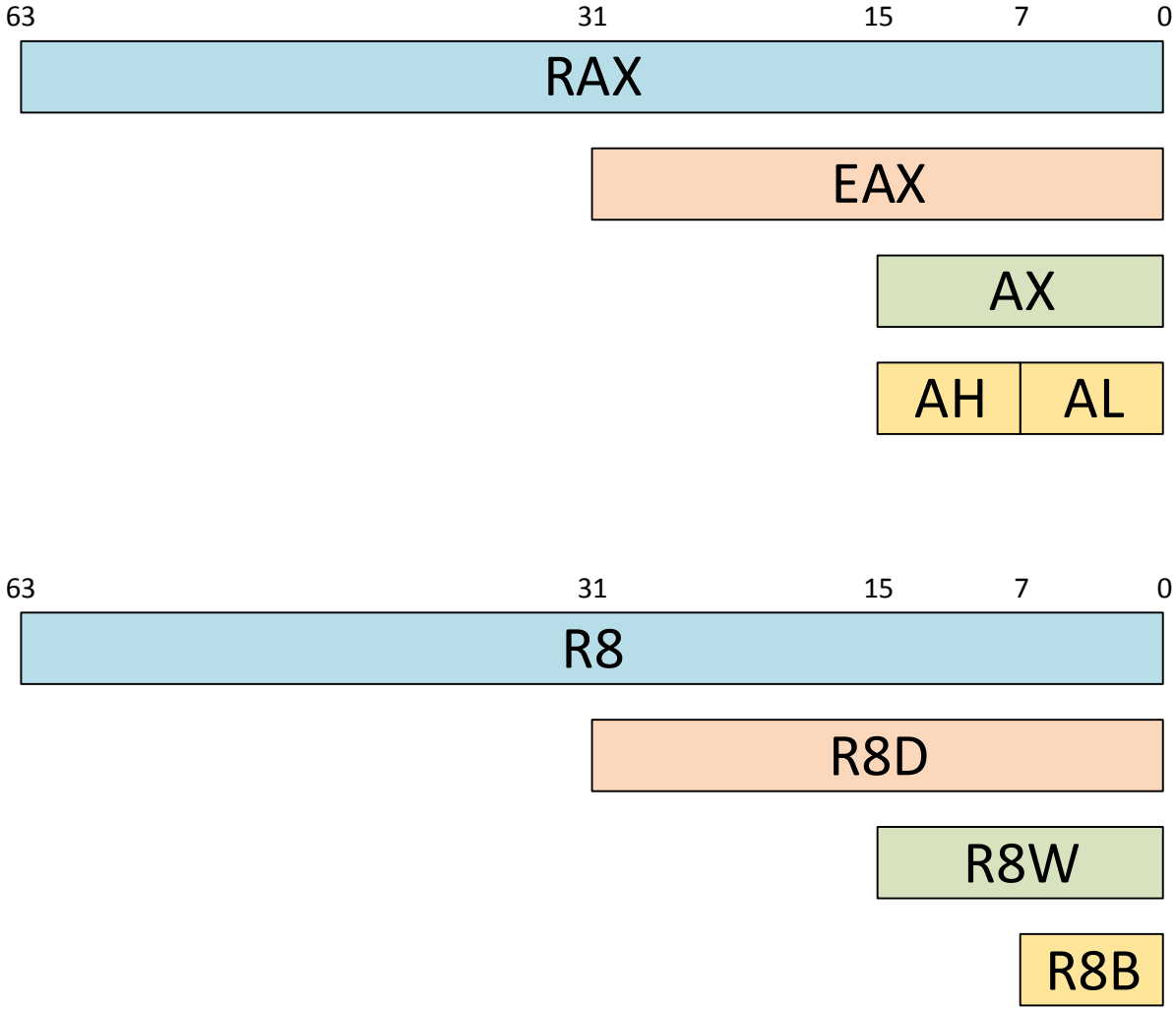
RAX
RCX
RDX
RBX
RSP
RBP
RSI
RDI
R8
R9
R10
R11
R12
R13
R14
R15

MMX0/FPR0
MMX1/FPR1
MMX2/FPR2
MMX3/FPR3
MMX4/FPR4
MMX5/FPR5
MMX6/FPR6
MMX7/FPR7

XMM0
XMM1
XMM2
XMM3
XMM4
XMM5
XMM6
XMM7
XMM8
XMM9
XMM10
XMM11
XMM12
XMM13
XMM15
XMM16

RIP
RFLAGS
IPR’s

x86 register Part naming



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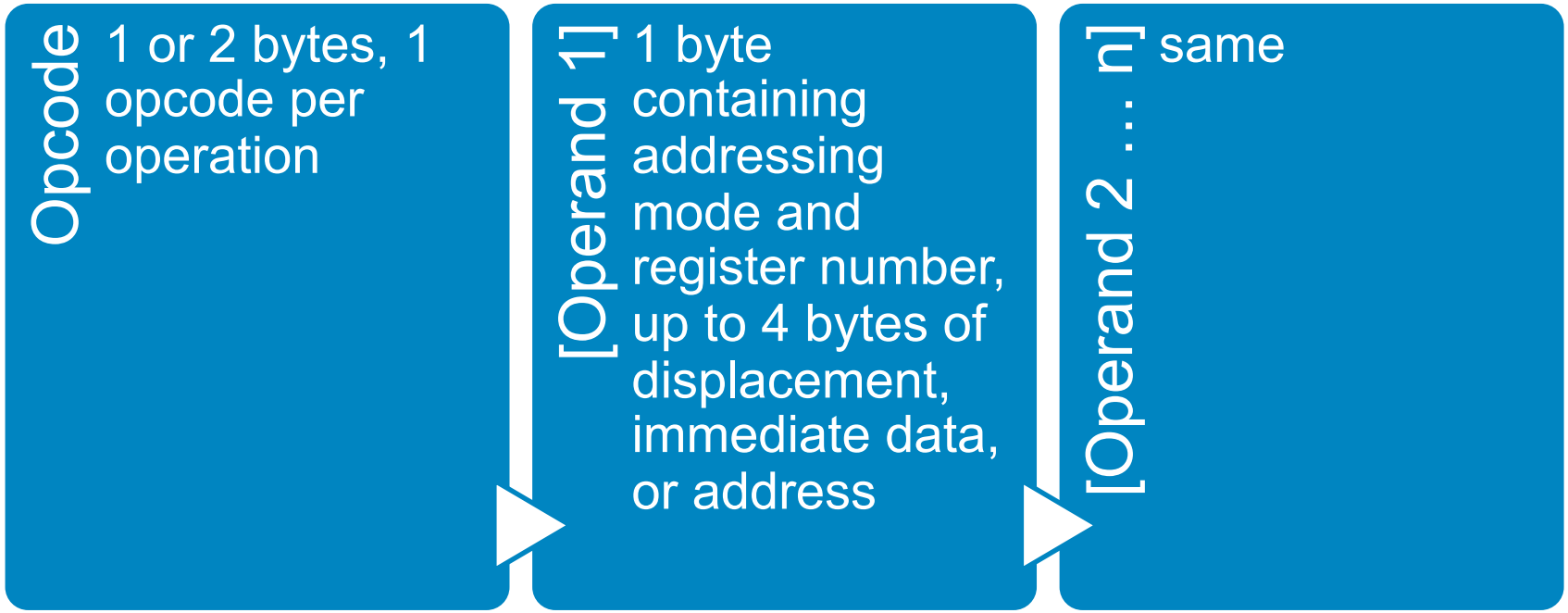
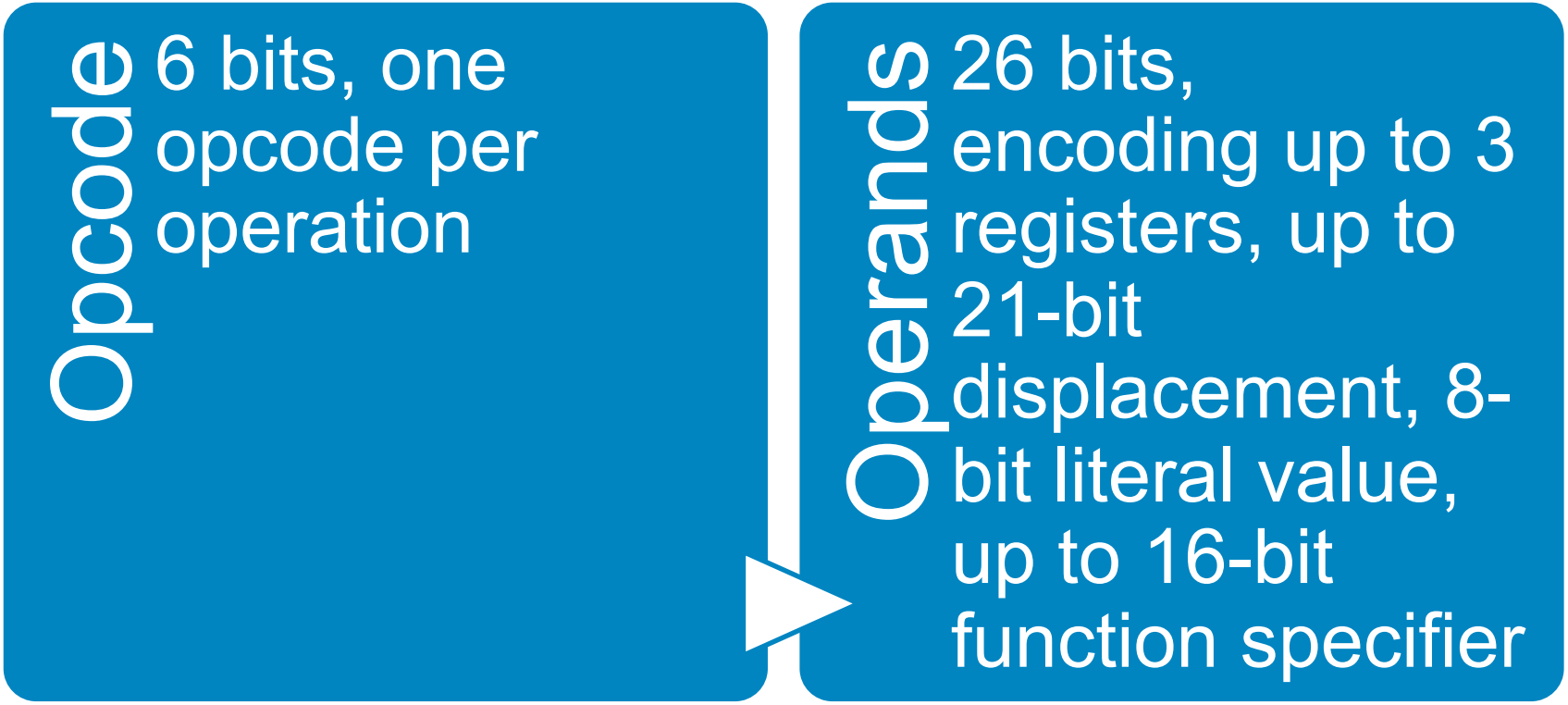
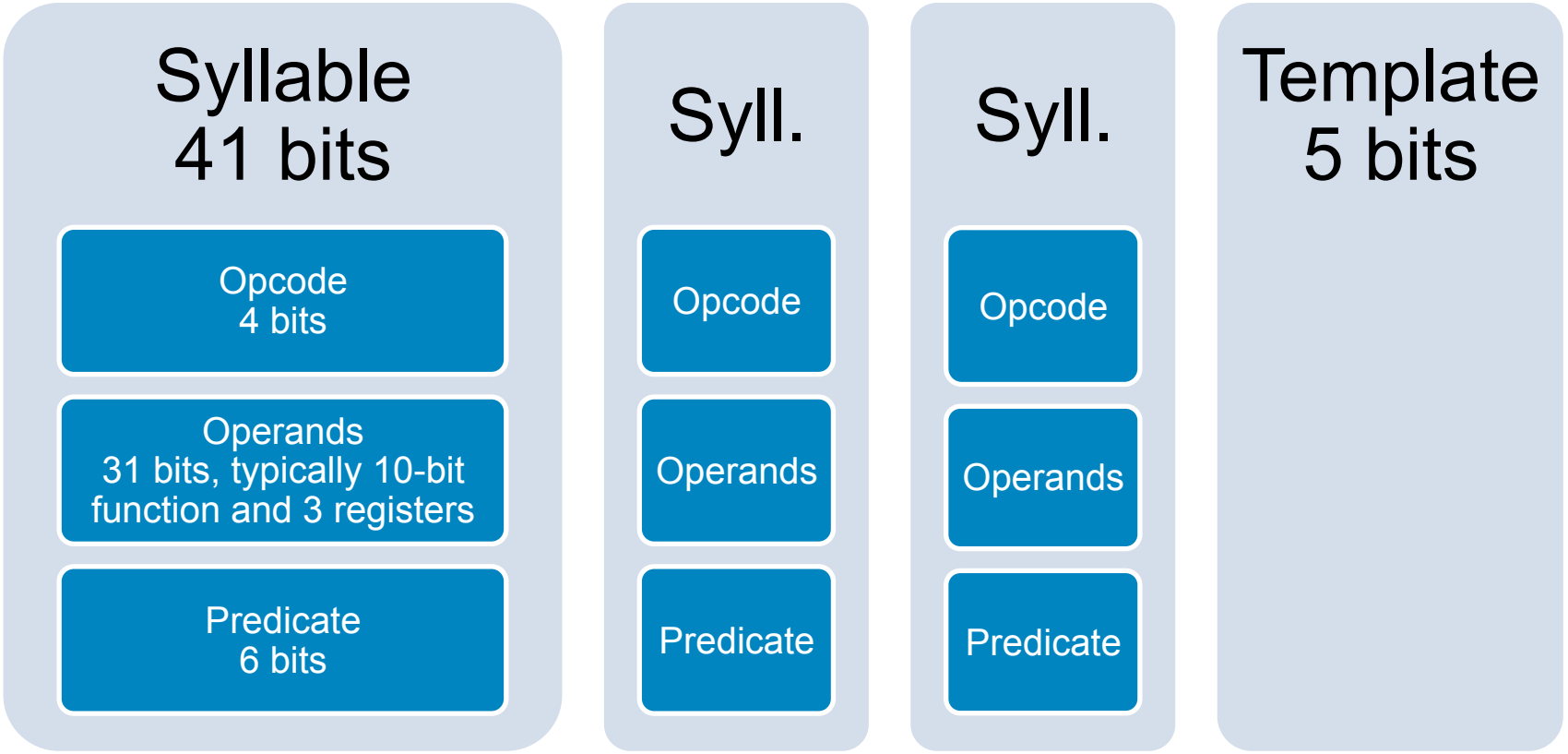
VAX Instruction encoding



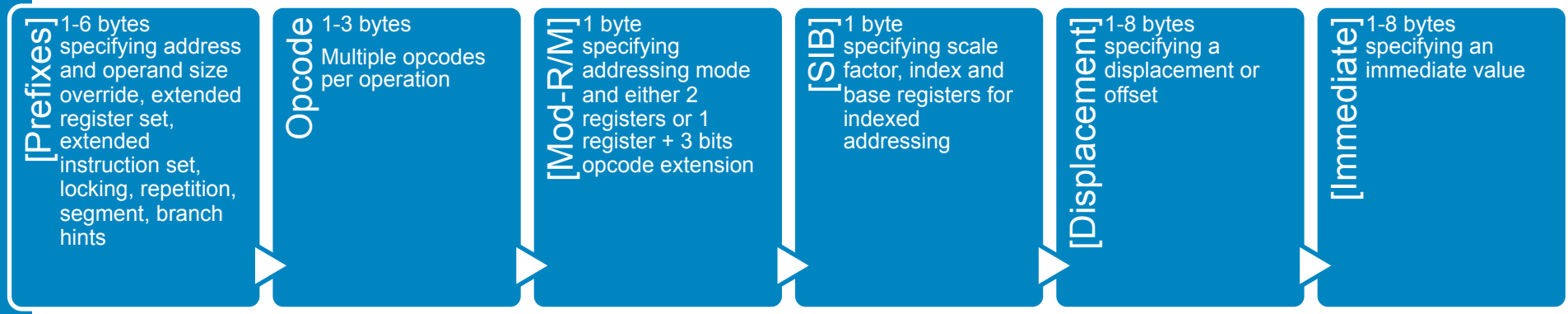
Alpha Instruction Encoding



Itanium Instruction Encoding



Intel x86 Instruction Encoding



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Memory Specs

	VAX	Alpha	Itanium	x86
Address size	32	64	64	64
Page size	512	8K/64K/512K/4M	4K-4G	4K/2M/1G
Split VA Space	no	yes	yes	yes
PT Levels	2	3	3	4
PTE Cache	no	no	VHPT	PDE cache
Virt. Addr. Size	32	48	54	48
Phys. Addr. Size	32	44	50	52 (48)
Segmentation	no	no	no	yes (kind of)
Prot. Bits in TLB	4 enc[KESU][RW]	11 [KESU][RW], FO[RWE]	7 enc[KESU], enc[RWX]	3 R/W, U/S, XD

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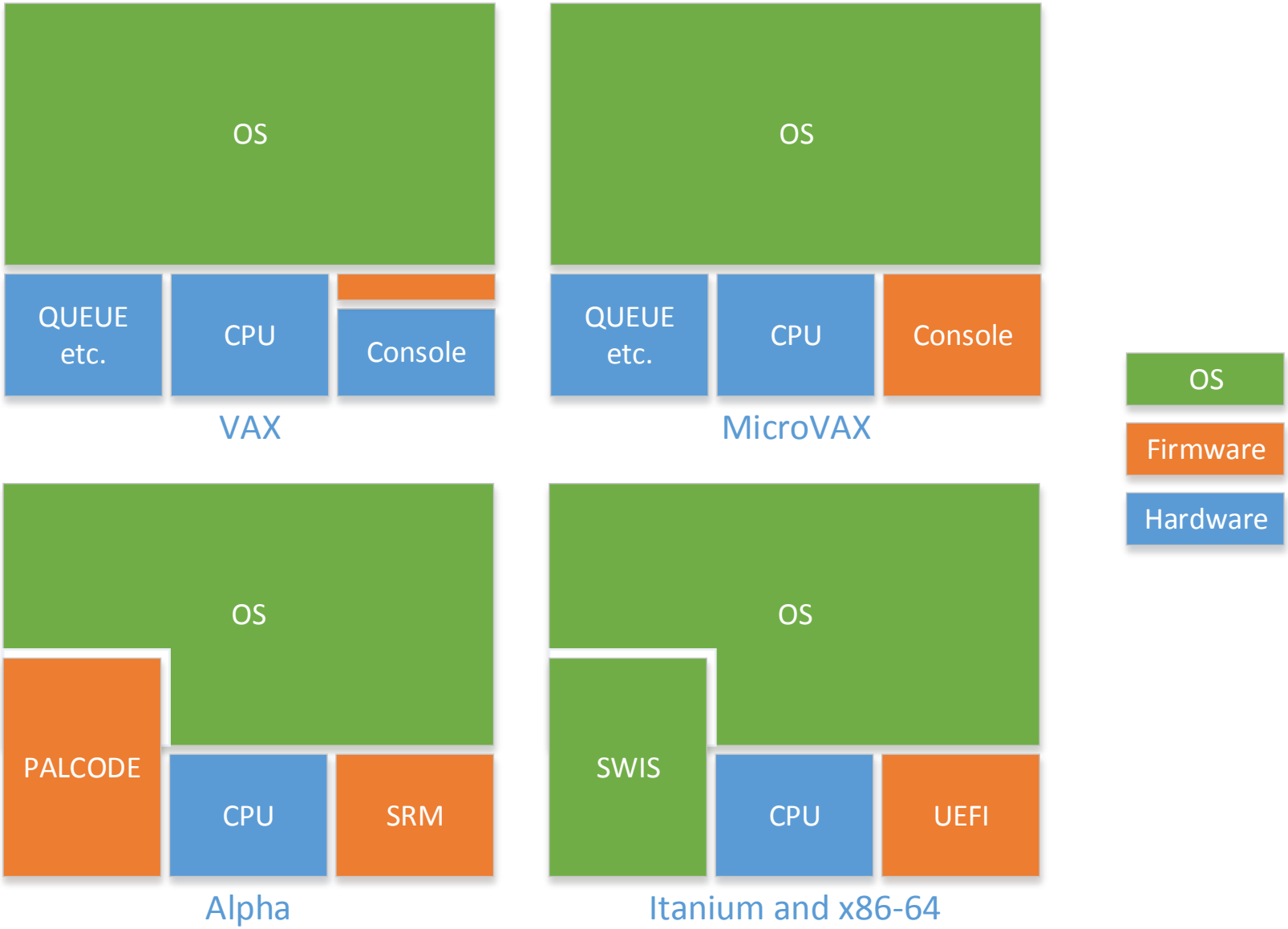
Hardware/Software Boundaries



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RAS Features in Itanium and Xeon

Feature	Itanium	Xeon
Cache ECC Coverage	✓	✓
Single-bit Memory Error Correction	✓	✓
Double-bit Memory Error Detection & Retry	✓	✓
ECC on Data Bus	✓	✓
Internal Logic Soft Error Checking	✓	Skylake-EX
Bad Data Containment	✓	✓
Intel Cache Safe	✓	✓
Memory Sparing	✓	✓
Memory Mirroring	✓	✓
Hot-Plug I/O	✓	✓
Memory Hot-Swap	✓	✓
Processor Lock-Step	✓	✓

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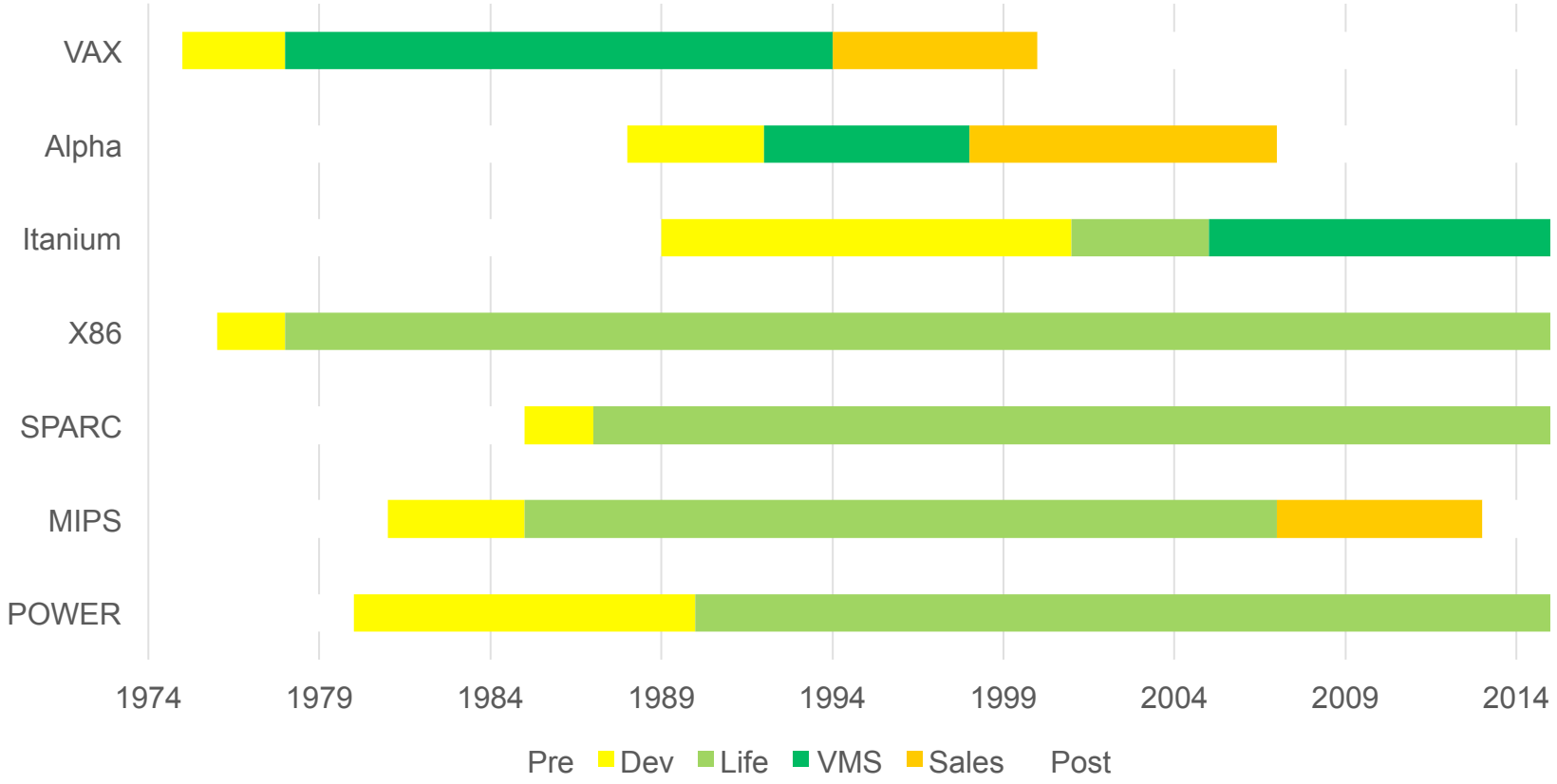
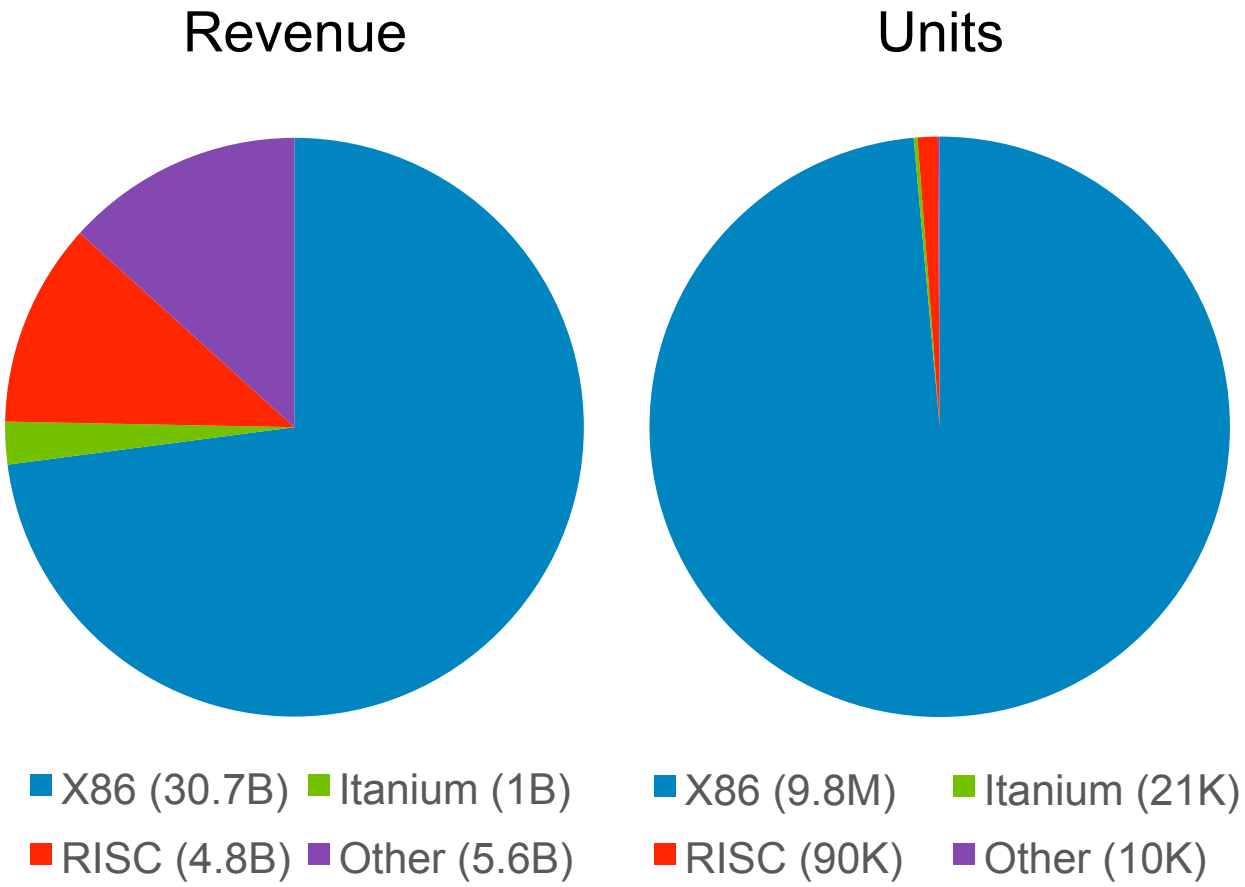
Lifespans of different architectures



2013 Server Market



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